

WHAT IS CLAIMED IS:

1. An apparatus, comprising:
 - a substrate having at least one trench wall;
 - a first layer;
 - a second layer wherein the first layer, the second layer and a portion of the substrate form a process stack, the first and second layers being a pull back distance from the trench wall thereby forming an implant region; and
 - a dopant in the implant region.
2. The apparatus according to claim 1, wherein the pull back distance is in a range from about 25 Å to about 300 Å.
3. The apparatus according to claim 1, wherein the pull back distance is substantially symmetrical about the second layer.
4. The apparatus according to claim 1, wherein the dopant in the implant region occupies the implant region in a concentration of about 1 part per million.
5. The apparatus according to claim 1, wherein the dopant has an implant energy in a preferred implant energy range from about 5 to about 25 keV.
6. An apparatus, comprising:
 - a substrate having at least one trench wall;
 - a first layer;
 - a second layer wherein the first layer, the second layer and a portion of the substrate form a process stack, the substrate further including a central area underneath the first layer having a threshold voltage that is about substantially uniform, the first and second layers being a pull back distance from the trench wall thereby forming an implant region; and
 - a dopant in the implant region.

7. The apparatus according to claim 6, wherein the dopant in the implant region changes an electrical characteristic of the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in the central area of the substrate underneath the first layer.

8. The apparatus according to claim 6, wherein the substrate further includes a corner region that comprises a part of the implant region, the corner region having a rounded contour.

9. An apparatus, comprising:

- a substrate having at least one trench wall;
- a first layer;
- a second layer wherein the first layer, the second layer and a portion of the substrate form a process stack, the first and second layers being a pull back distance from the trench wall thereby forming an implant region; and
- a dopant in the implant region and the substrate at the at least one trench wall.

10. The apparatus according to claim 9, wherein the substrate is a P-type substrate and the dopant is a P-type dopant.

11. The apparatus according to claim 9, wherein the substrate is an N-type substrate and the dopant is an N-type dopant.

12. The apparatus according to claim 9, wherein the dopant is one of Boron, Arsenic, Antimony, Indium, Phosphorous, and BF_2 .

13. The apparatus according to claim 9, wherein the dopant has an implant energy in a preferred implant energy range from about 5 to about 25 keV.

14. The apparatus according to claim 13, wherein the implant energy is in a more preferred implant energy range of less than or equal to about 10 keV.

15. An apparatus, comprising:

- a substrate having at least one trench wall;
- a first layer;
- a second layer wherein the first layer, the second layer and a portion of the substrate form a process stack, the first and second layers being a pull back distance from the trench wall thereby forming an implant region having a migration region; and
- a dopant in the implant and migration regions.

16. The apparatus according to claim 1, further comprising a third layer about the process stack.

17. An apparatus, comprising:

- a substrate having a surface and at least one trench wall;
- an oxide layer on the substrate;
- a nitride layer on the oxide layer wherein the oxide layer, the nitride layer and a portion of the substrate form a process stack extending away from the surface, the oxide layer and the nitride layer being a pull back distance from the trench wall thereby forming an implant region, the pull back distance being substantially symmetrical about the nitride layer; and
- a dopant in the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform.

18. The apparatus according to claim 17, wherein the pull back distance is in a range from about 25 Å to about 300 Å.

19. The apparatus according to claim 17, wherein the dopant is present in the substrate at the at least one trench wall.

20. The apparatus according to claim 17, wherein the at least one trench wall is angled in relation to the surface.

21. The apparatus according to claim 17, wherein the substrate further includes a corner region that comprises a part of the implant region, the corner region having a rounded contour.

22. The apparatus according to claim 17, wherein the implant region occupies a migration region adjacent to the oxide layer.

23. The apparatus according to claim 22, wherein the dopant occupies the migration region.

24. An apparatus having reduced transistor leakage attributes, comprising:
a substrate having a surface, a corner region and at least one trench wall;
an oxide layer on the substrate;
a nitride layer on the oxide layer wherein the oxide layer, the nitride layer and a portion of the substrate form a process stack extending away from the surface, the oxide layer and the nitride layer being a pull back distance in a range from about 25 Å to about 300 Å from the trench wall thereby forming an implant region, the pull back distance being substantially symmetrical about the nitride layer, the corner region of the substrate comprising a part of the implant region; and
a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform.

25. The apparatus according to claim 24, wherein the dopant is one of Boron, Arsenic, Antimony, Indium, Phosphorous and BF_2 .

26. The apparatus according to claim 24, wherein the corner region has a rounded contour.

27. The apparatus according to claim 24, wherein the implant region occupies a migration region adjacent to the oxide layer.

28. An transistor structure having reduced transistor leakage attributes, comprising:
a substrate having a surface, a corner region and at least one trench wall;
a transistor on the substrate, the transistor being formed from a process stack having:
an oxide layer on the substrate;
a nitride layer on the oxide layer; and
a portion of the substrate wherein the process stack extends away from the surface, the oxide layer and the nitride layer being a pull back distance in a range from about 25 Å to about 300 Å from the trench wall thereby forming an implant region, the pull back distance being substantially symmetrical about the nitride layer, the corner region of the substrate having a rounded contour and comprising a part of the implant region;
a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform; and
a third layer forming a plug in a shallow trench isolation of the substrate.

29. A method, comprising:

- providing a substrate;
- depositing a first layer;
- depositing a second layer;
- forming a trench wall in the substrate;
- forming an implant region by pulling back the first and second layers a pull back distance from the trench wall; and
- doping the implant region.

30. The method according to claim 29, wherein forming the implant region further includes pulling back the first and second layers the pull back distance in a range from about 25 Å to about 300 Å.

31. A product made by the method of claim 29.

32. A method, comprising:

- providing a substrate;
- depositing a first layer;
- depositing a second layer;
- forming a trench wall in the substrate;
- forming an implant region by pulling back the first and second layers a pull back distance from the trench wall; and
- doping the implant region resulting in raising a threshold voltage of the implant region.

33. The method according to claim 32, wherein raising the threshold voltage of the implant region further includes raising the threshold voltage to be about equivalent or greater than a threshold voltage of a central area of the substrate underneath the first layer.

34. The method according to claim 32, wherein doping the implant region further includes selecting a dopant from one of Boron, Arsenic, Antimony, Phosphorous, Indium, BF_2 , Indium then BF_2 , Indium then Boron, and Boron then BF_2 .

35. The method according to claim 32, wherein doping the implant region further includes implanting ions in a preferred implant energy range from about 5 to about 25 keV.

36. The method according to claim 32, wherein doping the implant region further includes doping in an angular orientation from about 0 to about 60° .

37. A product made by the method of claim 32.

38. A method, comprising:
providing a substrate;
depositing a first layer;
depositing a second layer;
forming a trench wall in the substrate;
forming an implant region by pulling back the first and second layers a pull back distance from the trench wall;
doping the implant region; and
migrating the implant region adjacent to the first layer.

39. The method according to claim 38, wherein doping the implant region further includes selecting a p-type dopant when the substrate is a p-type substrate.

40. The method according to claim 38, wherein doping the implant region further includes selecting an n-type dopant when the substrate is an n-type substrate.

41. The method according to claim 38, wherein forming an implant region further includes forming a rounded contour of a corner region of the substrate.

42. A method, comprising:

- providing a substrate;
- depositing a first layer;
- depositing a second layer;
- forming a trench wall in the substrate;
- forming an implant region by pulling back the first and second layers a pull back distance from the trench wall;
- doping the implant region; and
- doping the trench wall.

43. The method according to claim 42, wherein doping the implant region further includes doping the implant region to a thickness in a range from 200 Å to about 1000 Å.

44. A method of forming a structure, comprising:

- providing a substrate;
- depositing an oxide layer on the substrate;
- depositing a nitride layer on the oxide layer;
- forming a trench wall in the substrate wherein a process stack results that extends away from a surface of the substrate, the process stack including the oxide layer, the nitride layer and a portion of the substrate;
- forming an implant region by pulling back the first and second layers a pull back distance from the trench wall; and
- doping the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer.

45. The method according to claim 44, wherein doping the implant region further includes implanting ions in a preferred implant energy range from about 5 to about 25 keV.

46. The method according to claim 45, wherein implanting is in a more preferred implant energy range of less than or equal to about 10 keV.

47. The method according to claim 44, wherein forming an implant region further includes forming a rounded contour of a corner region of the substrate.

48. The method according to claim 44, wherein the method further includes doping the trench wall.

49. The method according to claim 44, wherein doping the implant region further includes selecting a dopant from one of Boron, Arsenic, Antimony, Phosphorous, Indium and BF_2 .

50. An isolation structure made by the method of claim 44.

51. A method of forming a transistor structure having reduced transistor leakage attributes, comprising:
 providing a substrate;
 depositing an oxide layer on the substrate;
 depositing a nitride layer on the oxide layer;
 forming a trench wall in the substrate wherein a process stack results that extends away from a surface of the substrate, the isolation stack comprising the oxide layer, the nitride layer and a portion of the substrate;
 forming an implant region by pulling back the first and second layers a pull back distance from the trench wall wherein a corner surface of the substrate, and a part of the implant region, having a rounded contour results;

doping the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the area of the substrate being about substantially uniform; and

replacing the oxide and nitride layers with a transistor.

52. The method according to claim 51, wherein the method further includes depositing a third layer on the process stack.

53. The method according to claim 52, wherein the method further includes planarizing the third layer.

54. The method according to claim 51, wherein replacing the oxide and nitride layers further includes wet etching the oxide and nitride layers away.

55. The method according to claim 51, wherein doping the implant region further includes implanting ions in a preferred implant energy range from about 5 to about 25 keV.

56. The method according to claim 51, wherein doping the implant region further includes selecting a dopant from one of Boron, Arsenic, Antimony, Phosphorous, Indium, BF_2 , Indium then BF_2 , Indium then Boron, and Boron then BF_2 .

57. A product made by the method of claim 51.

58. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device

includes

a substrate having at least one trench wall;
a transistor on the substrate, the transistor formed from a process stack having a
a first layer;
a second layer; and
a portion of the substrate, the first and second layers having been pulled back a pull back distance from the trench wall thereby forming an implant region; and
a dopant in the implant region.

59. The electronic system according to claim 58, wherein the pull back distance is in a range from about 25 Å to about 300 Å.

60. The electronic system according to claim 58, wherein the pull back distance is substantially symmetrical about the transistor.

61. The electronic system according to claim 58, wherein the substrate further includes a central area underneath the transistor having a threshold voltage that is about substantially uniform.

62. The electronic system according to claim 61, wherein the dopant in the implant region changes an electrical characteristic of the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in the central area of the substrate underneath the transistor.

63. The electronic system according to claim 58, wherein the substrate further includes a corner region that comprises a part of the implant region, the corner region having a rounded contour.

64. An electronic system, comprising:

- a processor; and
- a memory device coupled to the processor, wherein the memory device includes:
 - a substrate having at least one trench wall;
 - a transistor on the substrate, the transistor formed from a process stack having:
 - a first layer;
 - a second layer; and
 - a portion of the substrate, the first and second layers having been pulled back a pull back distance from the trench wall thereby forming an implant region; and
 - a dopant in the implant region and the substrate at the at least one trench wall.

65. The electronic system according to claim 64, wherein the substrate is a P-type substrate and the dopant is a P-type dopant.

66. The electronic system according to claim 64, wherein the substrate is an – type substrate and the dopant is an N-type dopant.

67. The electronic system according to claim 64, wherein the dopant in the implant region is present in a thickness range from about 200 Å to about 1000 Å.

68. The electronic system according to claim 64, wherein the dopant is one of Arsenic, Antimony, Indium, Phosphorous and BF_2 .

69. The electronic system according to claim 64, wherein the dopant has an implant energy in a preferred implant energy range from about 5 to about 25 keV.

70. The electronic system according to claim 69, wherein the implant energy is in a more preferred implant energy range of less than or equal to about 10 keV.

71. The electronic system according to claim 64, wherein the dopant in the implant region occupies the region in a concentration of about 1 part per million.

72. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device

includes:

a substrate having at least one trench wall;

a transistor on the substrate, the transistor formed from a process

stack having:

a first layer;

a second layer; and

a portion of the substrate, the first and second layers having been pulled back a pull back distance from the trench wall thereby forming an implant region having a migration region adjacent the transistor; and

a dopant in the implant region and the migration region.

73. The electronic system according to claim 72, wherein the substrate further includes a central area underneath the transistor having a threshold voltage that is about substantially uniform.

74. The electronic system according to claim 73, wherein the dopant in the implant region and the migration region changes an electrical characteristic of the implant region and the migration region thereby making a threshold voltage in the implant region and the migration region about equivalent to or greater than a threshold voltage in the central area of the substrate underneath the transistor.

75. An electronic system, comprising:

- a processor; and
- a memory device having reduced transistor leakage attributes coupled to the processor, wherein the memory device includes:
 - a substrate having a surface, a corner region and at least one trench wall;
 - a transistor on the substrate, the transistor formed from a process stack having:
 - an oxide layer on the substrate;
 - a nitride layer on the oxide layer; and
 - a portion of the substrate wherein the process stack extends away from the surface, the oxide layer and the nitride layer being a pull back distance in a range from about 25 Å to about 300 Å from the trench wall thereby forming an implant region, the pull back distance being substantially symmetrical about the nitride layer, the corner region of the substrate including a part of the implant region; and
 - a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the transistor layer, the threshold voltage of the central area of the substrate being about substantially uniform.

76. The electronic system according to claim 75, wherein the dopant is one of Boron, Arsenic, Antimony, Indium, Phosphorous and BF_2 .

77. The electronic system according to claim 75, wherein the corner region has a rounded contour.